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L4: Entry 38 of 55

File: JPAB

Jul 21, 1992

PUB-NO: JP404200238A

DOCUMENT-IDENTIFIER: JP 04200238 A

TITLE: POWER CONSUMPTION CONTROLLER AND POWER CONSUMPTION CONTROL METHOD OF  
COMMUNICATION SYSTEM

PUBN-DATE: July 21, 1992

## INVENTOR-INFORMATION:

NAME

COUNTRY

OKAMOTO, SHINJI

## ASSIGNEE-INFORMATION:

NAME

COUNTRY

MATSUSHITA ELECTRIC IND CO LTD

APPL-NO: JP02334721

APPL-DATE: November 29, 1990

INT-CL (IPC): H02J 3/00; H02J 13/00

## ABSTRACT:

PURPOSE: To suppress a power consumption to minimize the influence caused by stopping of respective equipments by detecting the power consumption of an equipment group and by placing an equipment with low operating priority in a stopped state, when the power consumption is detected to be higher than a predetermined one.

CONSTITUTION: A power consumption control equipment 1 monitors always the power consumption of the whole communication system by a power consumption detector 6. When the power consumption of the whole communication system is detected to be higher than the preset first value, respective consumed power control equipments 2-4 are instructed to stop a consumed power control equipment with the lowest power consumption priority level. Also thereafter, when the power consumption is detected to be higher than the first value, a temporary stop is instructed in order from a consumed power control equipment with low priority level. Thus, it is possible to suppress the power consumption and to minimize the influence caused by stopping of respective equipments because of stopping them in order from an equipment with low power consumption priority level.

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L36: Entry 6 of 12

File: JPAB

Dec 2, 1997

PUB-NO: JP409312935A

DOCUMENT-IDENTIFIER: JP 09312935 A

TITLE: POWER STORAGE TYPE POWER SUPPLY SYSTEM AND POWER STORAGE METHOD

PUBN-DATE: December 2, 1997

## INVENTOR-INFORMATION:

NAME	COUNTRY
FUJIMOTO, HIROYUKI	
YAMAMOTO, HIROSHI	
KAKAZU, TAKANORI	

## ASSIGNEE-INFORMATION:

NAME	COUNTRY
OSAKA GAS CO LTD	

APPL-NO: JP08127494

APPL-DATE: May 22, 1996

INT-CL (IPC): H02 J 3/32; H02 J 15/00

## ABSTRACT:

PROBLEM TO BE SOLVED: To improve the efficiency of a whole system and reduce an installed capacity.

SOLUTION: A power storage type power supply system has an AC generator 2 which generates an AC current supplied to a load 10, a battery 4 in which a power is stored, a converter 12 which converts the AC current from the AC generator 2 into a DC current, an inverter 14 which converts a DC current from the battery 4 into an AC current and a control means 22 which controls the converter 12 and the inverter 14. If the power consumption of the load 10 is smaller than a specified value, a part of the AC power from the AC generator 2 is stored in the battery 4. If the power consumption of the load 10 exceeds the specified value, the power stored in the battery 4 is supplied to the load 2.

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L4: Entry 48 of 55

File: DWPI

Nov 30, 2000

DERWENT-ACC-NO: 2001-096299

DERWENT-WEEK: 200111

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TITLE: Power consumption reduction apparatus for information processor, has power consumption control to cut power supply to processor when detected power consumption exceeds threshold value

## PATENT-ASSIGNEE:

ASSIGNEE	CODE
NEC GUNMA LTD	NIDE

PRIORITY-DATA: 1999JP-0144086 (May 24, 1999)

  

## PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<input type="checkbox"/> <a href="#">JP 2000330673 A</a>	November 30, 2000		004	G06F001/26

## APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP2000330673A	May 24, 1999	1999JP-0144086	

INT-CL (IPC): G06 F 1/26; G06 F 1/28; G06 F 1/32

ABSTRACTED-PUB-NO: JP2000330673A

## BASIC-ABSTRACT:

NOVELTY - Power consumption monitor (21) detects the fixed value of power supply to be supplied to information processor and compares it with the predetermined threshold value. Detecting signal is input to control unit (3) when the power consumption exceeds threshold value and the controller stops the power supply to the processor.

USE - Power consumption reduction apparatus is used for information processor.

ADVANTAGE - Sable drive can be obtained due to effective reduction in power supply consumption.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of power supply reduction apparatus.

Control unit 3

Power consumption monitor 21

CHOSEN-DRAWING: Dwg.1/4

TITLE-TERMS: POWER CONSUME REDUCE APPARATUS INFORMATION PROCESSOR POWER CONSUME  
CONTROL CUT POWER SUPPLY PROCESSOR Detect POWER CONSUME THRESHOLD VALUE

DERWENT-CLASS: T01

EPI-CODES: T01-L01;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N2001-073125

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## WEST Search History

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<i>DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L41	L40 same (threshold or value)	4
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<input type="checkbox"/>	L27	L26 and I9	3
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<input type="checkbox"/>	L22	((activat\$4 or start\$4 or initiat\$4 or begin\$4) near3 battery near2 discharg\$4) same ((based or depend\$4 or respons\$4) near3 power near2 (consum\$9 or usage or use))	0
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<input type="checkbox"/>	L17	L15 with battery	22
<input type="checkbox"/>	L16	L15 same battery	30

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<input type="checkbox"/>	L13	L12 same ((activat\$4 or start\$4 or initiat\$4 or begin\$4) near3 battery)	15
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<input type="checkbox"/>	L10	l3 and L9	9
<input type="checkbox"/>	L9	713/300,310,320,321,340.ccls.	2061
<input type="checkbox"/>	L8	(battery near5 discharg\$4) same l2	26
<input type="checkbox"/>	L7	(battery near5 discharg\$4) same l1	114
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		<i>DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>	
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<input type="checkbox"/>	L3	L2 same ((monitor\$4 or sens\$4 or detect\$4 or verif\$9 or check\$4 or determin\$4 or calculat\$4) near3 (threshold or value or watermark))	113
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<input type="checkbox"/>	L1	(control\$4 near5 power\$4 near5 consum\$9)	18548

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L4: Entry 14 of 55

File: USPT

Dec 26, 2000

DOCUMENT-IDENTIFIER: US 6167524 A

TITLE: Apparatus and method for efficient battery utilization in portable personal computers

## CLAIMS:

1. An apparatus for controlling power consumption of a computer system having a plurality of execution units comprising:

means for storing and retrieving a power efficiency value, and expected power consumption values corresponding to the plurality of execution units when said execution units are active;

means for determining which of said execution units are currently active;

means for calculating an approximate expected total power consumption value corresponding to said execution units when said execution units are active;

means for comparing said expected total power consumption value to said power efficiency value;

means for monitoring each of said execution units, and collecting said expected power consumption values;

means for canceling operation of said active execution units responsive to said means for comparing to control power consumption of the computer system, said canceling operation based on said calculated power consumption values and said power efficiency value; and,

means for setting a level of power allocation, wherein said power allocation correlates to said power efficiency value.

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L4: Entry 3 of 55

File: USPT

Apr 13, 2004

DOCUMENT-IDENTIFIER: US 6721894 B2

**\*\* See image for Certificate of Correction \*\***

TITLE: METHOD FOR CONTROLLING POWER OF A MICROPROCESSOR BY ASSERTING AND DE-ASSERTING A CONTROL SIGNAL IN RESPONSE CONDITIONS ASSOCIATED WITH THE MICROPROCESSOR ENTERING AND EXITING LOW POWER STATE RESPECTIVELY

**Brief Summary Text (14):**

In accordance with another embodiment of the presently claimed invention, a method for externally controlling a processor used to execute instructions for data processing, including: providing directly to the processor a power consumption control signal which includes first and second values by maintaining the first value in response to a detection of one or more conditions associated with initiation of a power consumption reduction procedure, and maintaining the second value in response to a detection of another one or more conditions associated with termination of the power consumption reduction procedure; and receiving an acknowledgement signal from the processor subsequent to an attainment of the first power consumption control signal value.

**CLAIMS:**

22. A method for externally controlling a processor used to execute instructions for data processing, comprising: providing directly to said processor a power consumption control signal which includes first and second values by maintaining said first value in response to a detection of one or more conditions associated with initiation of a power consumption reduction procedure, and maintaining said second value in response to a detection of another one or more conditions associated with termination of said power consumption reduction procedure; and receiving an acknowledgement signal from said processor subsequent to an attainment of said first power consumption control signal value.

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L32: Entry 3 of 3

File: USPT

Sep 25, 1990

DOCUMENT-IDENTIFIER: US 4959774 A

TITLE: Shadow memory system for storing variable backup blocks in consecutive time periods

Brief Summary Text (9):

A data storage system in accordance with the invention includes a volatile main memory coupled to a host CPU through a memory controller and a host CPU bus, a bus monitor circuit, a usage monitor memory, a power supply subsystem with battery backup and a shadow memory subsystem coupled to replicate in nonvolatile storage data stored by the main memory. By continually updating nonvolatile disk storage in the shadow memory subsystem to reflect changes in data stored by the volatile memory, the nonvolatile storage data remains nearly current with the volatile storage data. Upon the occurrence of a main utility power failure only a small portion of the main memory data capacity need be transferred to the nonvolatile store to produce a fully updated copy prior to power shutdown. As a result only a small amount of battery energy is required to complete the data backup in the event of a power failure and several rapid sequence power failures and restarts can be accommodated with practically sized backup batteries.

Detailed Description Text (13):

Power supply 54 includes the conventional transformer, rectification and filtering circuitry required to produce the DC voltage levels used throughout the data storage system 10. As long as adequate AC utility power is available from main power source 50 power supply 54 utilizes this available power. In the event of a main utility power failure, however, power supply 54 immediately begins extracting power from backup battery 56.

Detailed Description Text (14):

Power control circuit 58 receives the power from power supply 54 and distributes it to the remainder of the data storage system 10 under control of microprocessor system 24. In a conventional manner, power control circuit 58 switches the power provided to various components in the data storage system 10 as necessary to maintain normal operation. For example, while AC utility power is available all portions of the system are energized. However, while operating on backup power from battery 56, only those portions of the system required for a current operating mode are energized in order to conserve available backup energy. Upon completion of a battery energized data preservation mode following an AC power failure, microprocessor 24 provides to power control circuit 58 a PRESERVATION COMPLETE signal through connector bus 60. Power control circuit 58 responds to this PRESERVATION COMPLETE signal by terminating power to all portions of the data storage system 10 except power supply 54, the power control circuit 58 itself, and AC monitor circuit 52. This portion of the circuit consumes very little standby energy and the data storage system 10 is capable of surviving a utility power failure in excess of several days in duration. Upon resumption of utility power through main power source 50, AC power monitor 52 signals power control circuit 58 and microprocessor system 24 over connector bus 60. This signal causes power control circuit 58 to resume distribution of power to all parts of data storage system 10 and initiates a power on reset for microprocessor system 24 which then

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L23: Entry 1 of 5

File: USPT

Dec 7, 2004

DOCUMENT-IDENTIFIER: US 6828760 B2

TITLE: Electronic device that adjusts operation to accord with available power

Detailed Description Text (22):

If the decision of step 420 indicates that the battery of the electronic device does require charging, step 440 is performed in which the battery charger is activated. Step 450 is then performed in which the electronic device monitors the performance and adjusts the performance based on the current power consumption. Step 450 can include the dynamic increasing of the CPU performance in the event that the overall power consumption of the electronic device remains below a predetermined limit for a predetermined time. For example, in the event that the battery charger has completed charging the battery, thereby making additional power resources available for other functions within the electronic device, the power allocated to the CPU can be increased, thereby allowing the CPU to operate at increased performance. Step 460 is then performed in which the electronic device waits until another power adapter is interfaced. Step 460 represents the steady-state operation of the electronic device using the selected power adapter, or from an internal battery of the electronic device.

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L27: Entry 1 of 3

File: USPT

Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6714016 B2

TITLE: Method for displaying information concerning power consumption and electronic device

Abstract Text (1):

An intelligent battery pack in an electronic device such as a PC, sends such information as a voltage, a current, etc. related to power consumption to a controller via a line when the PC is driven by a battery. When the AC adapter is supplying electrical power to the device, the power source is changed to the battery pack once only during the measuring time so as to display data using both measuring and communicating functions of the battery pack. Consequently, no special electric power detector is provided in the power supply system of the AC adapter.

Brief Summary Text (2):

The present invention relates to a technique for displaying information concerning power consumption on a display in an electronic device driven by a battery, and more particularly to a technique for displaying information concerning power consumption with use of data received from an intelligent battery pack.

Brief Summary Text (11):

Under such circumstances, it is an object of the present invention to provide an electronic device driven by a battery and enabled to display information of its power consumption on a display screen. It is another object of the present invention to provide an electronic device driven by an intelligent battery pack enabling the sending of information concerning power consumption and enabled to display information concurring power consumption obtained from the battery pack on a display screen. It is still another object of the present invention to provide an electronic device driven by an AC adapter or intelligent battery pack and enabled to display information concerning power consumption on a display screen even when it is driven by any of the above power sources. It is still another object of the present invention to provide an electronic device driven by an intelligent battery pack or AC adapter and enabled to display information concerning power consumption on a screen with use of a simple means.

Brief Summary Text (18):

According to the present invention therefore, it is possible to provide an electronic device driven by a battery and enabled to display information concerning power consumption on its display screen. It is also possible to provide an electronic device driven by an intelligent battery pack that can send information concerning power consumption and enabled to display information concerning power consumption received from the battery pack. It is still possible to provide an electronic device driven by an AC adapter or intelligent battery pack and enabled to display information concerning power consumption regardless of the power source (AC adapter and intelligent battery pack). And, it is still possible to provide an electronic device driven by an intelligent battery pack or AC adapter and enabled to display information concerning power consumption with use of a simple means.

Current US Cross Reference Classification (4):

713/340

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L27: Entry 2 of 3

File: USPT

Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6126332 A

TITLE: Apparatus and method for automatically disconnecting address and data buses in a multimedia system when docking with a portable personal computer

Detailed Description Text (147) :

In order to conserve battery power the intelligent battery pack may enter low power consumption states when feasible. These could occur when the system is powered off or in rest mode. The intelligent battery pack must be able to sense when the computer enters a fully on state, or when the battery is being charged, and at that time return to normal sampling rates for its' sensors.

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L27: Entry 3 of 3

File: USPT

Feb 3, 1998

DOCUMENT-IDENTIFIER: US 5714870 A

TITLE: Method for measuring suspend-time power consumption in a battery-powered electronic device

Brief Summary Text (9):

While smart batteries have been used to monitor power consumption during operation of electronic devices, particularly in battery-powered computers, there presently is no way to monitor power consumption while a battery-powered computer is in a suspended condition. This is because a system host can only retrieve data from a smart battery when the system host is active. Determining suspend-time power consumption may be extremely advantageous, however, enabling users to avoid potentially-disastrous power outages during a suspend period. Such information may be applied, for example, to inform a user of how long a battery-powered device may remain suspended before the system fails due to insufficient battery power.

Detailed Description Text (24):

Upon being invoked again, ideally as close as possible to the time when host 1 is reactivated after being suspended, power consumption monitor 4 again determines the present capacity of battery 2 (Step 150) and the present reading of real-time clock 5 (Step 160). These values, representing a post-suspend battery charge capacity and a post-suspend time indicator, may then be compared to the pre-suspend values retrieved from non-volatile store 7 (Step 170) to calculate a value representing capacity loss/time (Step 180). Capacity loss/time may be calculated according to the following formula: ##EQU1## Power consumption monitor 4 saves the calculated capacity loss/time in non-volatile store 7, either in the same units returned by the respective smart battery functions used to determine the capacity and time values, or it may convert the value to other units depending upon the particular requirements of a given application. Other alternatives are possible as well.

Detailed Description Text (27):

In another embodiment of the present invention, power consumption monitor 4 may be used to provide predictive information to a user relating to how long host 1 may remain suspended without compromising system integrity due to insufficient capacity of battery 2. To do this, power consumption monitor 4 may invoke the AtRateTimeToEmpty() smart battery function. This is actually a two-part function, with the first part being an AtRate() function which may be used to establish a discharge rate. Power consumption monitor 4 may call AtRate() using a previously-stored value for capacity loss/time during suspend periods. A subsequent call to the AtRateTimeToEmpty() function with this AtRate() value returns a number of minutes host 1 can remain suspended before battery 2 is discharged.

Detailed Description Text (32):

The foregoing is a detailed description of particular embodiments of the present invention. The invention embraces all alternatives, modifications and variations that fall within the letter and spirit of the claims, as well as all equivalents of the claimed subject matter. For example, while the battery was described with reference to a so-called smart battery, capacity information can be obtained from standard batteries using known electronics techniques. In such a case, the power

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L11: Entry 1 of 2

File: USPT

Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6714016 B2

TITLE: Method for displaying information concerning power consumption and electronic device

Detailed Description Text (9) :

The controller 115 calculates an electric power value from both received current value and terminal voltage value. The electric power value is sent to the CPU via a line 133 and displayed on the display screen. The controller 115 calculates the power consumption of the PC from both discharged current value and terminal voltage value received respectively. However, the CPU 107 of the battery pack 103 may calculate the electric power so that the controller 115 receives the electric power value directly from the CPU 107. And, although the controller 115 sends an electric power value to the CPU of the PC 100, the controller 115 may send the discharged current value of the battery 105 to the CPU as a substitute value of the power consumption.

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L14: Entry 3 of 9

File: USPT

Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5808591 A

TITLE: Image display device, image display system and program cartridge used therewith

Detailed Description Text (123):

FIG. 53 shows one example of structure in which the controller 6 has a voltage monitoring function. In FIG. 53, the controller 6 includes a signal processing circuit 61 formed of shift register, a key input receiving portion 62, and a battery voltage monitoring circuit 63. The controller 6 includes a plurality of keys operated by a player, and the key input portion 62 produces key operation signals in correspondence with the operation of these keys. The signal processing circuit 61 captures the key operation signals for respective keys accepted at the key input receiving portion 62 when an instruction for reading the key input is provided from the CPU 221 in the body device 2, and outputs the signals serially to the CPU 221. The power-supply voltage monitoring circuit 63 always monitors reduction of output voltage of the battery box 8, and activates a 1-bit warning signal (to a high level, for example) when the value of the output voltage decreases to a predetermined value or lower. This warning signal is provided to the signal processing circuit 61. The signal processing circuit 61 outputs the provided warning signal to the CPU 221 together with the key operation signals. The CPU 221 performs certain warning operation when the warning signal from the controller 6 attains an active state. For example, it displays a message or a figure for prompting exchange of a battery on the screen. Also, it generates warning for prompting exchange of a battery from a speaker 228. Or, an indicator for warning may be provided in the body device 2, which will emit light or may be driven.

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L16: Entry 3 of 30

File: USPT

Feb 22, 2000

DOCUMENT-IDENTIFIER: US 6029049 A

TITLE: Wireless selective call receiver with speech notice function in which power supply voltage is determined in loading state

Brief Summary Text (9):

The reception antenna 1 receives a radio signal which is transmitted from a base station. The radio section 2 demodulates the radio signal which is received by the reception antenna 1. The decoder control unit 3 compares the demodulated signal A and an own call number of the wireless selective call receiver. When the demodulated signal A is coincident with the own call number, the decoder control unit 3 stores a message signal B subsequent to the call number of the demodulated signal A in the message memory section 4. Also, the decoder control unit 3 outputs a coincidence signal E to the display output control unit 5. The reset switch 12 generates a trigger for starting or stopping the display. The display output control unit 5 issues a control signal F to the message memory section 4 in response to the trigger from the reset switch such that the stored message signal C is sent out to a display driver 6 and displayed on the display unit 7, when the coincidence signal E has been received from the decoder control unit 3. The power supply section 11 composed of a dry battery cell or a charged battery cell of 1.05 V to 1.5 V and the DC/DC converter 10 converts the output voltage of the power supply section 11 into a predetermined voltage. The output voltage of the DC/DC converter 10 is supplied to each of sections of the wireless selective call receiver. The low voltage determining section 8 performs a low voltage determination of the output voltage from the power supply section 11 for every predetermined time interval, using a timer 9. When the output voltage from the power supply section 11 decreases to a value lower than a predetermined level, a signal H indicative of the determining result of the low voltage is outputted from the low voltage determining section 8 to the display output control unit 5. In this case, a low voltage caution operation is started.

Detailed Description Text (22):

As described above, according to the present invention, the wireless selective call receiver of this example with the speech notice function is composed of the low voltage determining means for determining whether or not the output voltage of the power supply section decreases from the predetermined value, the speech synthesizing and amplifying means for converting the reception message which has been stored in the memory section into the speech signal, and for amplifying it such that it is outputted as the speech from the speaker, the speech output control means for performing the power supply voltage supply control of the speech synthesizing and amplifying means and an speech output control. Because the output voltage value of the power supply section is determined to perform the execution or stop of the speech output, after the predetermined time period of the S timer elapses from when the supply of the power supply to the speech synthesizing and amplifying means is started, in a case where an speech output is to be performed, it is possible to make a system be stable without changing the lifetime of the battery cell of the power supply section in the reception wait state in which an speech output is not performed. Also, in the wireless selective call receiver which can operate with one battery cell, there is an excellent effect that the system of the wireless selective call receiver in a new field of the wireless selective call receiver with the speech notice function which needs a large current.

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L4: Entry 4 of 55

File: USPT

Apr 6, 2004

DOCUMENT-IDENTIFIER: US 6717434 B2

TITLE: Logic circuit module having power consumption control interface and a recording medium storing the module

## CLAIMS:

3. A logic circuit module having a built-in main processor, comprising: a consumption power request status register which loads a consumption power request issued from another logic circuit module; and a consumption power control register which controls a consumption power of the other logic circuit module, wherein said processor: periodically monitors a value of said consumption power status register, sets a value of said consumption power control register to a proper value in accordance with the value of said consumption power status register, and supplies a proper clock signal and power to the other logic circuit module in accordance with the set value in said consumption power control register.

4. A logic circuit module having a built-in main processor, comprising: a consumption power request status register which loads a consumption power request issued from another logic circuit module; and a consumption power control register which controls a consumption power of the other logic circuit module, wherein said processor: periodically monitors a value of said consumption power status register, sets a value of said consumption power control register to a proper value in accordance with the value of said consumption power status register, and controls a clock generator circuit and power existing in an external of the logic circuit module in accordance with the set value in said consumption power control register.

8. A storage medium storing a logic circuit module implemented by a built-in main processor, wherein the logic circuit module functionally comprises: a consumption power request status register for loading a consumption power request issued from another logic circuit module; and a consumption power control register for controlling a consumption power of the other logic circuit module, wherein the processor: periodically monitors a value of said consumption power status register, setting a value of said consumption power control register to a proper value in accordance with the value of said consumption power status register, and supplies a proper clock signal and power to the other logic circuit module in accordance with the set value in said consumption power control register, or controls a clock generator circuit and power outside of the logic circuit module in accordance with the set value in said consumption power control register.

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L4: Entry 5 of 55

File: USPT

Feb 17, 2004

DOCUMENT-IDENTIFIER: US 6694443 B1

TITLE: SYSTEM FOR CONTROLLING POWER OF A MICROPROCESSOR BY ASSERTING AND DE-ASSERTING A CONTROL SIGNAL IN RESPONSE TO CONDITION ASSOCIATED WITH THE MICROPROCESSOR ENTERING AND EXITING LOW POWER STATE RESPECTIVELY

Brief Summary Text (16):

In accordance with another embodiment of the presently claimed invention, power management control circuitry for coupling to a processor used to execute instructions for data processing, the power management control circuitry being external to the processor and including control circuitry and acknowledgement circuitry. The control circuitry, for coupling to the processor provides directly to the processor a power consumption control signal that: includes first and second values; maintains the first value in response to a detection of one or more conditions associated with initiation of a power consumption reduction procedure; and maintains the second value in response to a detection of another one or more conditions associated with termination of the power consumption reduction procedure. The acknowledgement circuitry, for coupling to the processor, receives an acknowledgement signal from the processor subsequent to an attainment of the first power consumption control signal value.

Brief Summary Text (18):

In accordance with another embodiment of the presently claimed invention, power management control circuitry for coupling to a processor used to execute instructions for data processing, the power management control circuitry being external to the processor and including control means and acknowledgement means. The control means is for providing directly to the processor a power consumption control signal that: includes first and second values: maintains the first value in response to a detection of one or more conditions associated with initiation of a power consumption reduction procedure; and maintains the second value in response to a detection of another one or more conditions associated with termination of the power consumption reduction procedure. The acknowledgement means is for receiving an acknowledgement signal from the processor subsequent to an attainment of the first power consumption control signal value.

## CLAIMS:

36. An apparatus including power management control circuitry for coupling to a processor used to execute instructions for data processing, said power management control circuitry being external to the processor and comprising: control circuitry, for coupling to said processor, that provides directly to said processor a power consumption control signal that includes first and second values, maintains said first value in response to a detection of one or more conditions associated with initiation of a power consumption reduction procedure, and maintains said second value in response to a detection of another one or more conditions associated with termination of said power consumption reduction procedure; and acknowledgement circuitry, for coupling to said processor, that receives an acknowledgement signal from said processor subsequent to an attainment of said first power consumption control signal value.

50. An apparatus including power management control circuitry for coupling to a